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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,802	08/04/2004	Amy J. Gottschc	BUR920030165US1	4801

7590 02/06/2007

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EXAMINER	
TABONE JR, JOHN J	
ART UNIT	PAPER NUMBER
2138	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/710,802	GOTTSCHE ET AL.	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 November 2007 and 04 August 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-19 are currently pending in the application and have been examined. Claims 2, 3, 12 and 18 have been amended.

2. The objection to the drawings in item 3 on page 2 of the previous Office action of record have been withdrawn by the Examiner. Applicants failed to amend Fig. 1 to add descriptive labels and to increase the margins to Fig. 2. It is noted, however, that sufficient margins have been added to Fig. 1. Therefore, the objections to the drawings in items 2 and 4 on page 2 of the previous Office action of record are maintained as provided below.

3. The claim objections are withdrawn by the Examiner due to Applicants' amendments filed 11/24/2006.

Response to Arguments

4. Applicant's arguments filed 11/24/2006 have been fully considered but they are not persuasive.

In response to the Applicants' arguments pertaining to claim 19 as outlined on page 9, 5th paragraph, the Examiner is not persuaded by these arguments. The Examiner would like to point out that claim 19 was stated as being rejected in the Office Action Summary Form PTOL-326, paragraph 6 (i.e. claims 1-19 are rejected) as well as being rejected with claim 1 on page 4 of the previous Office action of record. The Examiner further contends that this clerical error in the Office action did not affect

Applicants' ability to reply to the rejection of this claim. If it did, the Applicants' were required to notify the Office within one (1) month of the mailing of the Office action. See MPEP 710.06. Therefore, the arguments are not persuasive.

As per the arguments for independent claim 1:

In response to Applicants' arguments concerning claim 1 the Examiner would first like to point out that "the claim as a whole must be considered". MPEP 2141.02. In light of this, the Examiner contends that the limitation "coupling the at least one segment having the first set of vectors including the varied at least one vector" would strongly suggest that the claimed at least one segment contains a group of vectors including the first initial vector. Thus, the Examiner asserts that the argued limitation "defining at least one segment within the first initial vector" only relates the first initial vector with the at least one segment not that the segments are within the first initial vector as the Applicants' contend. Based on this interpretation, the Examiner asserts that Gruodis teaches the argued limitation "defining at least one segment within the first initial vector" (Col. 3, ll. 49-62) as set forth in the previous Office action of record and presented below. As established above the claimed at least one segment contains a group of vectors including the first initial vector. As such, Gruodis's vector alignment circuit 30 offsets or delays the vectors within the segments (Col. 11, ll. 30-45, delays the sixteen output vectors). Therefore, the Examiner asserts that Gruodis teaches "offsetting the first initial vector a predetermined amount within the at least one segment".

The above presented arguments renders Applicants' argument for claim 10 moot.

It is the Examiner's conclusion that independent claim 1 is not patentably distinct or non-obvious over the prior arts of record namely, Gruodis et al. (US-6092225). Therefore, the rejection is maintained. Based on their dependency on independent claim 12, claims 3-11 stand rejected. Furtherer, in the absence of arguments concerning claim 19, the rejection is maintained.

As per the arguments for independent claim 12:

Applicants' argue on page 13, "Theodoseau does not disclose the counter control [402] forming a control bit definition file and does not disclose the counter control configured to be added to the at least one vector". The Examiner does not agree with Applicants' contentions and asserts that Theodoseau does disclose the counter control [402] is "formed in a control bit definition file" in that the invention provides for emulation of hardware signal pattern generators (i.e. files in software) and additionally providing full selectivity of function (including driving or signal detection) for any channel, fully selectable correlation of channels with pins and full selectivity of clocking, waveform, phase, and waveform convention on each channel. The Examiner also asserts that Theodoseau further discloses "the counter control [402] is configured to be added to the at least one vector" in that a system and method are provided for specifying a counting function of each of a plurality of counters, providing ordered nesting of counting of the plurality of counters, developing logic signals from outputs of the plurality of counters, specifying a waveform convention in accordance with each of the logic signals, and outputting a vector as an input to an integrated circuit in accordance with the logic

signals and the waveform convention. (Col. 4, ll. 8-14, 22-30). The Examiner further asserts that the vector tables in cols. 9-11 clearly show the counter control bits added to each vector.

Applicants' argue on page 14, "Theodoseau does not disclose combining the macro, control bit, pattern formats, and global definition files to form a final vector to produce a final pattern". The Examiner asserts that Theodoseau teaches the above cited limitation in that [a]ll of these operations cause generation of vectors under control of the write macro and timing element 425 (which also provides for inclusion (combining) of stability and set-up vectors and the refresh macro) by sequencing through loops previously specified for counters A-F as depicted at 550 of FIG. 5 which is carried out after the input to timing element 425 has been completed. (Col. 15, ll. 22-29).

It is the Examiner's conclusion that independent claim 12 is not patentably distinct or non-obvious over the prior arts of record namely, Theodoseau (US-5872797). Therefore, the rejection is maintained. Based on their dependency on independent claim 12, claims 13-18 stand rejected.

Drawings

5. The drawings are objected to because descriptive labels other than numerical are needed for Fig. 1. See 37 CFR 1.84(o).

6. The drawings are objected to because of insufficient margins for Fig. 2. See 37 C.F.R. § 1.84(g).

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-11 and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Gruodis et al. (US-6092225), hereinafter Gruodis.

Claim 1 and 19:

Gruodis teaches defining a first initial vector (**a set of four vectors at the start of each cycle**) and defining at least one segment within the first initial vector (A test is organized into a succession of test cycles with **each test cycle being subdivided into four segments**). (Col. 3, ll. 49-62). Gruodis also teaches offsetting the first initial vector

a predetermined amount (**vector alignment circuit 30**) within the at least one segment. (Col. 3, ll. 56-60, col. 5, ll. 22-32, col. 11, ll. 30-45). Gruodis further teaches defining a counter loop comprising loops of the first initial vector within the at least one segment to produce a first set of vectors in accordance with the counter loop, defining a progressively changing variation of the first initial vector for each loop of the counter loop so at least one vector of the first set of vectors varies from the first initial vector and coupling the at least one segment having the first set of vectors including the varied at least one vector to produce a final pattern for a circuit under test. (Col. 4, l. 10 to col. 6, l. 51).

Claim 2:

Gruodis teaches selecting a predefined vector pattern. (Col. 4, ll. 10-14).

Claim 3:

Gruodis teaches defining a first initial vector further comprises at least one of running a vector, delaying a vector, rerunning a vector [or] looping a vector. (Col. 4, l. 10 to col. 6, l. 51).

Claim 4:

Gruodis teaches overriding the first initial vector with a second vector. (Col. 8, ll. 21-24).

Claim 5:

Gruodis teaches selecting an input pin on a device to be tested for the first initial vector. (Col. 3, ll. 49-52).

Claim 6:

Gruodis teaches defining a name for the input pin on the device to be tested (**Tester 10 includes a set of J tester channels CH1 through CHJ, each connected to a separate pin of an integrated circuit device under test (DUT) 12**). (Col. 3, ll. 49-52, col. 13, l. 55 to col. 14, l. 21).

Claim 7:

Gruodis teaches defining a counter, and looping the first initial vector a prescribed number of times in accordance with the counter. (Col. 4, l. 10 to col. 6, l. 51).

Claim 8:

Gruodis teaches defining a data control vector (**vector forming a "subroutine sequence, col. 6, ll. 27-43**) to allow a prescribed input format of the first initial vector. (Col. 4, l. 10 to col. 6, l. 51).

Claim 9:

Gruodis teaches defining a new format vector (**supplied by the vector formatter 16**) to be added to the first initial vector to reconfigure the shape of the first vector. (Col. 4, l. 10 to col. 6, l. 51, col. 11, ll. 30-45).

Claim 10:

Gruodis teaches defining a second vector, allocating a second segment configured to contain the second vector and offsetting the second vector a predetermined amount within the second segment. (Col. 3, ll. 49-62, col. 3, ll. 56-60, col. 5, ll. 22-32, col. 11, ll. 30-45, col. 4, l. 10 to col. 6, l. 51).

Claim 11:

Gruodis teaches defining a counter loop comprising loops of the second vector within the second segment to produce a second set of vectors having a prescribed number of vectors in accordance with the counter loop defining a progressively changing variation of the second vector for each loop of the counter loop so at least one vector of the second set of vectors varies from the second vector and outputting the second segment having the second set of vectors as per the rejection of claim 1 is repeated via the looping commands. (Col. 4, l. 10 to col. 6, l. 51).

8. Claims 12-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Theodoseau (US-5872797), hereinafter Theodoseau.

Claim 12:

Theodoseau teaches selecting a macro definition file (**read macro 406, write macro 404**) defining at least one vector, forming a control bit definition file (**counter control 402**) configured to be added to the at least one vector, creating a pattern definition file (**pattern control selector 420**) configured to selectively alter a portion of the at least one vector, creating a global definition file (**refresh macro 408 includes write array, read array and variable retention testing**) configured to alter the entire vector and combining the macro, control bit, pattern formats, and global definition files to form a final vector to produce a final pattern (**The macros then build a plurality of patterns which are stored in memory 430 and read out in sequence, when called**). (Col. 6, l. 36 to col. 9, l. 50, Col. 15, ll. 22-29).

Claim 13:

Theodoseau teaches repeating the final pattern in accordance with a counter range. (Col. 7, ll. 39-51, Fig. 5).

Claim 14:

Theodoseau teaches forming setup vector files (**start-up vectors 414**) configured to power-up a device under test. (Col. 7, ll. 9-38, col. 11, ll. 49-58).

Claim 15:

Theodoseau teaches forming stability vectors files (**stability vectors 412**) configured to stabilize a device under test between actual test signals. (Col. 7, ll. 9-38, col. 11, ll. 49-58).

Claim 16:

Theodoseau teaches outputting the final pattern to a device under test. (Col. 6, l. 36 to col. 9, l. 50).

Claim 17:

Theodoseau teaches creating multiple final patterns and adding the multiple final patterns to one another. (Col. 19, l. 49 to col. 11, l. 40).

Claim 18:

Theodoseau teaches at least one of any one of overlapping, delaying, mixing, and offsetting at least two of the multiple final patterns. (Col. 6, l. 36 to col. 9, l. 50).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

John J. Tabone, Jr. 2/1/07
Examiner
Art Unit 2138

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